REMARKS

This Amendment responds to the Office Action dated March 5, 2004 in which the Examiner required a new title, objected to claims 3, 6 and 8 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form and rejected claims 1, 2, 4, 5 and 7 under 35 U.S.C. §102(e).

As indicated above, a new title has been provided which clearly indicates the invention to which the claims are directed. Applicants respectfully request the Examiner approves the new title.

As indicated above, minor typographical informalities in the abstract, claim 5 and specification have been corrected. Applicants respectfully request the Examiner approves the corrections.

As indicated above, claims 1, 4 and 7 have been amended to make explicit what is implicit in the claim. Applicants respectfully submit that the amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claims.

Claim 1 claims a trace data control circuit comprises a branch event generation circuit, a CPU-access event generation circuit, a selection means, a memory means and a trace data abbreviation means. The branch event generation circuit is for outputting trace data related to a branch instruction in response to a branch instruction. The CPU-access event generation circuit is for outputting a trace data related to a data access instruction in response to a data access instruction. The selection means is capable of inputting at least trace data output from the branch-event generation circuit and trace data output from the CPU-access event generation circuit, and selects trace data related to either one of these events. The

memory means is for storing the trace data. The trace data abbreviation means abbreviates one part of the trace data and outputs the partly abbreviated trace data excluding the abbreviated part of the trace data. The branch event generation circuit further comprises an address abbreviation information generation means detecting an overlapped portion of a branch-source address with a branch-destination address from the upper address bit sides thereof, and generating a branch-destination address abbreviation information.

Through the structure of the claimed invention having a trace data abbreviation means which outputs trace data excluding an abbreviated part of the trace data, as claimed in claim 1, the claimed invention provides a trace data control circuit capable of tracing the operation of a CPU in real time. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claim 4 claims a trace data control circuit comprises a branch event generation circuit, a CPU-access event generation circuit, a selection means, a memory means and a trace data abbreviation means. The branch event generation circuit is for outputting trace data related to a branch instruction in response to a branch instruction. The CPU-access event generation circuit is for outputting a trace data related to a data access instruction in response to a data access instruction. The selection means is capable of inputting at least trace data output from the branch-event generation circuit and trace data output from the CPU-access event generation circuit, and selecting trace data related to either one of these events. The memory means is for storing the trace data, and a trace data abbreviation means that abbreviates one part of the trace data and outputs the trace data without the abbreviated part of the trace data. The CPU-access event generation circuit further

comprises an address abbreviation information generation means detecting an overlapped portion of a preceding address to be accessed with a succeeding address to be accessed next from the upper address bit sides thereof, in the case of consecutive data access operation, and generating succeeding address abbreviation information.

Through the structure of the claimed invention having a trace data abbreviation means which abbreviates one part of the trace data and outputs the trace data without the abbreviated part of the trace data, as claimed in claim 4, the claimed invention provides a trace data control circuit which is capable of tracing the operation of the CPU in real time while operating at a faster rate by reducing cycle time. The prior art does not show, teach or suggest the invention as claimed in claim 4.

Claim 7 claims a trace data control circuit comprises a branch event generation circuit, a CPU-access event generation circuit, a selection means, a memory means and a trace data abbreviation means. The branch event generation circuit is for outputting trace data related to a branch instruction in response to a branch instruction. The CPU-access event generation circuit is for outputting a trace data related to a data access instruction in response to a data access instruction. The selection means is capable of inputting at least trace data output from the branch-event generation circuit and trace data output from the CPU-access event generation circuit, and selects trace data related to either one of these events. The memory means is for storing the trace data. The trace data abbreviation means abbreviates one part of the trace data and outputs the trace data without the abbreviated part of the trace data. The CPU-access event generation circuit further

comprises one or more than one latching means for latching read or write data per predetermined number of bits respectively, one or more than one comparing means each for comparing bit strings held by the one or more than one latching means per predetermined number of bits with a predetermined abbreviation target bit string, and a data abbreviation information generation circuit that inputs the result of the comparison output from the one or more than one comparing means and generates abbreviation information per predetermined number of bits of data related to the read or write data.

Through the structure of the claimed invention having a trace data abbreviation means that abbreviates one part of the trace data and outputs the trace data without the abbreviated part as claimed in claim 7, the claimed invention provides a trace data control circuit which is capable of tracing the operation of a CPU in real time and in which the number of data packets of the trace data can be reduced to speed up the output operation thereof. The prior art does not show, teach or suggest the invention as claimed in claim 7.

Claims 1, 2, 4, 5 and 7 were rejected under 35 U.S.C. §102(e) as being anticipated by *Edwards et al* (U.S. Patent No. 6,684,348).

Edwards et al appears to disclose that the trace information may be compressed by the trace system. By compressing information, trace information is preserved for transmission over lower-bandwidth links and maximizes on-chip trace storage. (col. 2, lines 41-44) In one aspect, the integrated circuit includes circuitry that compressed the trace information by representing at least one of an operand address, program counter, bus analyzer and instruction addresses as a signed address offset relative to the at least one address; and representing timing

information by a time difference. In one embodiment, address offsets are determined by subtracting a previously sent address from a new address. (col. 4, lines 22-29) FIGS. 11A and 11B show compressed data formats in accordance with one embodiment. To minimize the size of trace messages sent over external links and to maximize storage of trace messages, trace messages may be compressed. For example, program counter addresses and bus analyzer addresses may be compressed. An encoding method may be used whereby either one or two bytes are used to represent signed address offsets of either 7- or 14-bits, these offsets being relative to the previous address of the same type. If the address cannot be expressed as a 7-bit or a 14-bit offset value, an absolute 32-bit value may be encoded instead. (col. 18, lines 45-56)

Thus, *Edwards et al* merely discloses compressing trace information by address offsets which are determined by subtracting a previously sent address from a new address. Nothing in *Edwards et al* shows, teaches or suggests a trace data abbreviation means which outputs trace data without an abbreviated part of the trace data as claimed in claims 1, 4 and 7. Rather, *Edwards et al* merely discloses compressing trace data as address offsets which are determined by subtracting a previously sent address from a new address.

Since nothing in *Edwards et al* shows, teaches or suggests a trace data abbreviation means which abbreviates one part of the trace data and outputs the trace data without the abbreviated part as claimed in claims 1, 4 and 7, applicants respectfully request the Examiner withdraws the rejection to claims 1, 4 and 7 under 35 U.S.C. §102(e).

Claims 2 and 5 depend from claims 1 and 4 and recite additional features. Applicants respectfully submit that claims 2 and 5 would not have been anticipated by *Edwards et al* within the meaning of 35 U.S.C. §102(e) at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 2 and 5 under 35 U.S.C. §102(e).

Since objected to claims 3, 6 and 8 depend from allowable claims, applicants respectfully request the Examiner withdraws the objection thereto.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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